TITLE

Semiconductor Device Voltage Supply for a System With at Least Two, Especially Stacked, Semiconductor Devices

[0001] This application claims priority to German Patent Application DE 10315303.9, which was filed April 2, 2003.

TECHNICAL FIELD

[0002] The invention relates to a system with two - especially stacked - semiconductor devices and a semiconductor device voltage supply for such a system, respectively.

BACKGROUND

[0003] Semiconductor devices, in particular memory devices such as DRAMS (DRAM = Dynamic Random Access Memory or dynamic read-write-memory, respectively) in general comprise one or several voltage supply means.

[0004] A voltage supply means serves to generate, from an - externally provided - voltage, a voltage used internally in the semiconductor device.

[0005] The voltage level of the internal voltage generated by the semiconductor device voltage supply means may differ from the level of the external voltage.

[0006] In particular, the internally used voltage level may be lower than the externally used voltage level.

[0007] An internal voltage level that is reduced vis-à-vis the externally used voltage level has, for instance, the advantage that the power loss in the semiconductor device can be reduced.

[0008] Furthermore, the external voltage may be subject to relatively strong fluctuations. Therefore, a so-called voltage regulator is frequently used as voltage supply means, which - in order that the device may be operated without fault - converts the external voltage into an internal voltage that is subject to relatively minor fluctuations only and is regulated at a particular, constant (possibly reduced) value.

[0009] Conventional voltage regulators may, for instance, comprise a differential amplifier and a field effect transistor. The gate of the field effect transistor may be connected to an output of the differential amplifier, and the source of the field effect transistor may e.g. be connected to the external voltage.

[0010] A reference voltage - which is subject to relatively minor fluctuations only - is applied to the positive input of the differential amplifier. The voltage output at the drain of the field effect transistor may be fed back to the negative input of the differential amplifier directly, or e.g. by the interposition of a voltage divider.

[0011] The differential amplifier regulates the voltage available at the gate connection of the field effect transistor such that the (fed back) drain voltage - and thus the voltage output by the voltage regulator - is constant and as high as the reference voltage, or e.g. by a certain factor higher.

[0012] Semiconductor devices are usually incorporated in appropriate housings, e.g. appropriate surface mountable housings (SMD housings) or plug mountable housings (e.g. corresponding Dual-In-Line (DIL) housings, Pin-Grid-Array (PGA) housings, etc.).

[0013] In one single housing, there may also be arranged two or more semiconductor devices instead of only one single semiconductor device.

[0014] In the case of memory devices, in particular DRAMs for increasing the storage density, several semiconductor devices may, for instance, be mounted in a stacked manner in one single housing.

[0015] For instance, two 256 Mbit memory devices may be provided in one single housing, this effecting a 512 Mbit chip.

[0016] The semiconductor devices, in particular memory devices, provided in one single housing comprise voltage supply means that are independent of one another.

[0017] When a memory device is accessed (i.e. when corresponding external data are stored on the memory device, or when data that are stored on the memory device are read

out), there will flow, in general, relatively high currents that are generated by the corresponding voltage supply means.

[0018] Contrary to this, only relatively low currents will flow in standby or refresh operation (e.g. for supplying leakage currents or operating currents).

[0019] The standby or refresh currents each may, for instance, be in the range of approx. 50 μA - i.e. amount to a total of 100 μA in the case of e.g. two stacked memory devices (with the operating currents of the respective voltage supply means constituting the major part of these currents).

BRIEF SUMMARY OF THE INVENTION

[0020] It is an object of the invention to provide a novel system with two - especially stacked - semiconductor devices, and - in particular - a semiconductor device voltage supply for such a system, respectively.

[0021] The invention achieves this and further objects by the subject matter of claim 1.

[0022] Advantageous further developments of the invention are indicated in the subclaims.

[0023] In accordance with a basic idea of the invention, a system, in particular a semiconductor device system, is provided, comprising

[0024] - a first semiconductor device, and

[0025] - a second semiconductor device,

[0026] wherein the first semiconductor device comprises a voltage supply means, and wherein the voltage supply means of the first semiconductor device is connected to the second semiconductor device, so that the voltage supply means of the first semiconductor device can provide a supply voltage for the second semiconductor device.

[0027] It is of particular advantage when the second semiconductor device additionally also comprises a voltage supply means.

[0028] Preferably, in a first operating mode of the second semiconductor device, the voltage supply means of the second semiconductor device provides the voltage supply for the second semiconductor device, and in a second operating mode of the second

semiconductor device - in particular in a standby or refresh mode -, this is effected by the voltage supply means of the first semiconductor device.

[0029] The voltage supply means of the second semiconductor device may then be deactivated, so that the operating current thereof may be saved (and thus, altogether, the currents required for operating the semiconductor devices).

[0030] In an advantageous development of the invention, the first semiconductor device and the second semiconductor device are arranged in one and the same housing.

[0031] Preferably, the first and second semiconductor devices are arranged in the housing in a stacked manner.

[0032] Advantageously, the housing may be a plug mountable semiconductor device housing, or e.g. a surface mountable semiconductor device housing.

[0033] It is particularly preferred when the first and/or the second semiconductor devices are corresponding memory devices, in particular corresponding DRAM memory devices.

[0034] In an advantageous development of the invention, the voltage supply means of the first semiconductor device is connected to a corresponding pad of the first semiconductor device.

[0035] Preferably, the pad of the first semiconductor device is connected to a corresponding pad of the second semiconductor device, which the voltage supply means of the second semiconductor device can be connected to.

[0036] The pad of the first semiconductor device may, for instance, be connected directly to the corresponding pad of the second semiconductor device, in particular by means of an appropriate bonding wire.

[0037] Alternatively, the pad of the first semiconductor device may, for instance, also be connected to the corresponding pad of the second semiconductor device indirectly, e.g. via an interposer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0038] In the following, the invention will be explained in detail by means of several embodiments and the enclosed drawing. The drawing shows:

[0039] Figure 1a is a schematic representation of a system with two stacked semiconductor devices with a semiconductor device voltage supply in accordance with a first embodiment of the present invention; and

[0040] Figure 1b is a schematic representation of a system with two stacked semiconductor devices with a semiconductor device voltage supply in accordance with a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0041] List of Reference Signs

[0042] 1 semiconductor device system

[0043] 2a semiconductor device

[0044] 2b semiconductor device

[0045] 3a voltage supply means

[0046] 3b voltage supply means

[0047] 4 semiconductor device housing

[0048] 5a semiconductor device pad

[0049] 5b semiconductor device pad

[0050] 5c semiconductor device pad

[0051] 5d semiconductor device pad

[0052] 6 bonding wire

[0053] 6a bonding wire

[0054] 6b bonding wire

[0055] 7a line

[0056] 7b line

[0057] 7c line

[0058] 7d line

[0059] 8 activating/deactivating control means

[0060] 9 interposer

[0061] 10 connection

[0062] Figure 1a is a schematic representation of a system 1 with two stacked semiconductor devices 2a, 2b in accordance with a first embodiment of the present invention.

[0063] The two semiconductor devices 2a, 2b are - apart, in particular, from the components serving for voltage supply of the semiconductor devices 2a, 2b or controlling the voltage supply, respectively, which will be explained in more detail in the following - substantially of identical structure.

[0064] The semiconductor devices 2a, 2b may, on principle, be any type of logic and/or memory devices, e.g. functional memory devices, in particular programmable logic devices (PLDs) or programmable logic arrays (PLAs), or e.g. table memory devices, in particular ROM or RAM table memory devices, etc.

[0065] For instance, appropriate DRAM table memory devices, e.g. a 256 Mbit, a 512 Mbit, or a 1 Gbit DRAM table memory device 2a, 2b, for instance appropriate DDR-DRAMs (Double Data Rate DRAMs), may be used as semiconductor devices 2a, 2b.

[0066] As is illustrated schematically in Figure 1a, the semiconductor devices 2a, 2b are arranged in the same semiconductor device housing 4.

[0067] The housing 4 may, for instance, be an appropriate plug mountable semiconductor device housing, e.g. a Dual-In-Line (DIL) housing, a Pin-Grid-Array (PGA) housing, etc., or a surface mountable semiconductor device housing (SMD housing), etc.

[0068] As results further from Figure 1a, the semiconductor devices 2a, 2b are mounted in the housing 4 such that they are substantially stacked.

[0069] By the stacking of the semiconductor devices 2a, 2b in the same housing 4, the system 1 can - e.g. when two 256 Mbit memory devices 2a, 2b are used as semiconductor devices 2a, 2b - altogether be used as a 512 Mbit memory device (or e.g. when two 512 Mbit memory devices are used, as a 1 Gbit memory device, etc.).

[0070] As is further illustrated in Figure 1a, each semiconductor device 2a, 2b comprises a voltage supply means 3a, 3b having a structure similar to that of conventional voltage supply means (or – alternatively - a plurality of, e.g. two, three, four, five, six, or seven, voltage supply means having a structure corresponding to that of the voltage supply means 3a, 3b).

[0071] The voltage supply means 3a, 3b serve to generate, from an external voltage - provided by a voltage source (not illustrated) arranged externally of the semiconductor devices 2a, 2b and of the housing, respectively - a corresponding internal voltage - used, for instance, internally in the respective semiconductor device 2a, 2b (cf. explanations below).

[0072] The external voltage provided by the external voltage source may, for instance, be supplied to the voltage supply means 3a, 3b via one or a plurality of supply pins (not illustrated) of the semiconductor device housing 4, and via semiconductor device pads connected therewith (e.g. the pads 5c, 5d illustrated in Figure 1a), as well as via corresponding lines 7a, 7b connected to the pads 5c, 5d or extending in the semiconductor devices 2a, 2b, respectively.

[0073] As voltage supply means 3a, 3b, e.g. appropriate charge pumps may be used that have a structure similar to that of conventional charge pumps, or e.g. - as in the embodiment illustrated here - voltage regulating means 3a, 3b that have a structure similar to that of conventional voltage regulating means.

[0074] These means serve to convert the external voltage - which may be subject to relatively strong fluctuations--into the above-mentioned internal voltage - which is subject to relatively minor fluctuations only and is regulated at a particular, constant value.

[0075] The internal voltage may, for instance, have substantially the same, or alternatively e.g. a lower, voltage level as/than the external voltage. The external voltage may, for instance, lie in the range of between 1.5 V and 2.5 V, e.g. at 1.8 V, and the internal voltage e.g. in the range of between 1.3 V and 2.0 V, e.g. at 1.5 V.

[0076] The voltage supply means 3a, 3b or voltage regulating means 3a, 3b, respectively, each may, for instance, comprise a differential amplifier and a field effect transistor. The gate of the field effect transistor may be connected to an output of the differential amplifier, and the source of the field effect transistor may be connected e.g. to the above-mentioned external voltage.

[0077] A reference voltage that is subject to relatively minor fluctuations only is applied to the positive input of the differential amplifier. The voltage output at the drain of the field effect transistor may be fed back to the negative input of the differential amplifier directly, or e.g. by the interposition of a voltage divider.

[0078] The differential amplifier regulates the voltage available at the gate connection of the field effect transistor such that the (fed back) drain voltage - and thus the voltage output by the corresponding voltage supply means 3a, 3b or voltage regulating means 3a, 3b, respectively, e.g. at corresponding lines 7c, 7d or connections, respectively (i.e. the above-mentioned voltage used internally on the semiconductor devices 2a, 2b (internal voltage)) - is constant and as high as the reference voltage, or e.g. by a certain factor higher.

[0079] The first and the second semiconductor devices 2a, 2b are operated in several, different modes.

[0080] In a first mode (working mode), an external access to the first or second semiconductor device 2a, 2b may, for instance, be effected (similar as with conventional memory devices). In so doing, corresponding – external - data may, for instance, be stored on the first or second semiconductor device 2a, 2b (with the data being input e.g. at corresponding pins of the semiconductor device housing 4), or data stored on the first or second semiconductor device 2a, 2b may be read out externally (with the data being output at corresponding pins of the semiconductor device housing 4).

[0081] A second operating mode may, for instance, be a standby mode (similar as with conventional memory devices), or, e.g. a refresh mode (also similar as with conventional memory devices).

[0082] During a refresh mode (or more exactly: during a refresh operation), the capacitors of the memory cells on which the data stored on the semiconductor devices 2a, 2b are stored, are correspondingly refreshed.

[0083] A refresh cycle may be performed at regular time intervals, e.g. every 1 to 10 ms or every 10 to 1000 ms, etc.

[0084] As will be explained in more detail in the following, in the semiconductor device system 1 illustrated in Figure 1a, the voltage supply means 3b of the second semiconductor device 2b is activated in the above-mentioned first operating mode (and possibly in one or several further operating mode(s)) - e.g. during the above-mentioned working mode -, and in the above-mentioned second operating mode (and possibly in one or several further operating mode(s)) - e.g. during the standby mode and/or during the refresh mode - the voltage supply means 3b of the second semiconductor device 2b is deactivated.

[0085] This happens e.g. by corresponding activating/deactivating signals being fed to the voltage supply means 3b of the second semiconductor device 2b by an activating/deactivating control means 8.

[0086] In the activated state, the voltage supply means 3b of the second semiconductor device 2b is switched on (is, in particular, connected to the supply or external voltage, so that corresponding operating currents - e.g. of between 20 μA and 80 μA, e.g. 50 μA - are flowing), and in the deactivated state it is switched off (is, in particular, separated from the supply or external voltage, so that corresponding operating currents are prevented from flowing).

[0087] As is further illustrated in Figure 1a, the voltage supply means 3a of the first semiconductor device 2a is connected - here: via the line 7c - to a corresponding semiconductor device pad 5a of the first semiconductor device 2a.

[0088] The pad 5a is connected to a corresponding semiconductor device pad 5b of the second semiconductor device 2b by means of a bonding wire 6.

[0089] The pad 5b of the second semiconductor device 2b is connected - here: via the line 7d - to the voltage supply means 3b of the second semiconductor device 2b (or to a line or a connection, respectively, at which - in the activated state of the voltage supply means 3b of the second semiconductor device 2b - the internal voltage then generated thereby is output).

[0090] By the above-described connection of the voltage supply means 3a of the first semiconductor device 2a to the second semiconductor device 2b it is achieved that, in the above-mentioned second operating mode of the second semiconductor device 2b (and possibly in one or several further operating mode(s)) - e.g. during the standby mode and/or during the refresh mode -, the voltage supply means 3a of the first semiconductor device 2a can, in addition to the – internal - supply voltage (internal voltage) for the first semiconductor device 2a, provide the – internal - supply voltage (internal voltage) for the second semiconductor device 2b.

[0091] In other words, in the above-mentioned second operating mode the voltage supply means 3a of the first semiconductor device 2a generates the respectively required (internal) voltages for both semiconductor devices 2a, 2b - the voltage supply means 3b of the second semiconductor device 2b is deactivated, so that the operating current thereof may be saved (this, altogether, reducing the currents required for operating the semiconductor devices 2a, 2b).

[0092] Contrary to this--as has already been explained above - in the above-mentioned first operating mode of the second semiconductor device 2b (and possibly in

one or several further operating mode(s)) - e.g. during the working mode - the voltage supply means 3b of the second semiconductor device 2b is put to an active state (and the voltage supply means 3a of the first semiconductor device 2a is possibly additionally separated from the voltage supply means 3b of the second semiconductor device 2b, or the above-mentioned line or the connection, respectively, at which the voltage supply means 3b of the second semiconductor device 2b outputs the internal voltage generated thereby (e.g. by controlling the activating/deactivating control means 8, or alternatively e.g. a corresponding control means provided on the first semiconductor device 2a)).

[0093] By this it is achieved that, in the above-mentioned first operating mode of the second semiconductor device 2b (and possibly in one or several further operating mode(s))--e.g. during the first working mode - the voltage supply means 3b of the second semiconductor device 2b provides the - internal - supply voltage (internal voltage) for the second semiconductor device 2b (and the voltage supply means 3a of the first semiconductor device 2a the – internal - supply voltage (internal voltage) for the first semiconductor device 2a).

[0094] Advantageously, the first and the second semiconductor devices 2a, 2b are - in particular until passing through the device function adjusting step which will be explained in more detail in the following - (at first) of substantially identical structure.

[0095] By means of the device function adjusting step it is determined during the manufacturing of the semiconductor devices whether a corresponding semiconductor device is to fulfill a function that corresponds to the function of the above-mentioned first semiconductor device 2a, i.e. the function of a "master" which, in the above-mentioned second operating mode (and possibly in one or several further operating mode(s)), is to

provide - in addition to its own voltage supply - the respectively required (internal) voltage also for one or several further semiconductor device(s), or a function corresponding to the function of the above-mentioned second semiconductor device 2b, i.e. the function of a "slave" which is to obtain, in the above-mentioned second operating mode (and possibly in one or several further operating mode(s)) the respectively required (internal) voltage from another semiconductor device ("master").

[0096] For determining the function of a corresponding semiconductor device, an appropriate device function adjusting means, in particular an appropriate fuse, may be provided on the semiconductor devices.

[0097] An appropriate laser fuse or e.g. an appropriate electrical fuse may, for instance, be used as a fuse.

[0098] When the fuse is shot, the corresponding device assumes e.g. a "master" function, and otherwise a "slave" function (or vice versa).

[0099] As is shown by means of the alternative embodiment for a semiconductor device system 1 illustrated in Figure 1b, the voltage supply means 3a of the first semiconductor device 2a may also be connected in any other way than in that illustrated in Figure 1a to the second semiconductor device 2b (or more exactly: the voltage supply means 3b of the second semiconductor device 2b (or the line or the connection, respectively, at which the voltage supply means 3b of the second semiconductor device 2b outputs the internal voltage generated thereby in the activated state).

[0100] For instance, in accordance with Figure 1b, the voltage supply means 3a of the first semiconductor device 2a may be connected - as described above - to a

semiconductor device pad 5a of the first semiconductor device 2a which - other than with the embodiment illustrated in Figure 1a - is connected to a corresponding contact of an interposer 9 (or to a corresponding leadframe connection 10 of the housing 4) by means of a bonding wire 6.

[0101] The interposer contact (or the leadframe connection 10) is connected to the pad 5b of the second semiconductor device 2b by means of a further bonding wire 6b, which is connected to the voltage supply means 3b of the second semiconductor device 2b (or the above-mentioned line or the connection, respectively, at which - in the activated state of the voltage supply means 3b of the second semiconductor device 2b - the internal voltage then generated thereby is output).

[0102] By this it can be achieved--similar as with the embodiment illustrated in Figure 1a - that in the second operating mode of the second semiconductor device 2b (e.g. during the standby mode and/or during the refresh mode) the voltage supply means 3a of the first semiconductor device 2a can - in addition to the voltage supply (internal voltage) for the first semiconductor device 2a - also provide the supply voltage (internal voltage) for the second semiconductor device 2b.

[0103] When - corresponding to the first embodiment - the voltage supply means 3b of the second semiconductor device 2b is correspondingly deactivated in the second operating mode, the operating current of the voltage supply means 3b can - corresponding to the embodiment illustrated in Figure 1a- be saved in the above-mentioned second operating mode (and thus, altogether, the currents required for operating the semiconductor devices 2a, 2b).

der Unterseite herstellen. Dadurch kann die Zahl der erforderlichen Durchkontaktierungen 10 im Trägersubstrat 1 reduziert werden. Eine weitere Funktion der Anschlußelemente 11 und 12 ist die Ableitung der in dem Multi-Chip-Modul entstehenden Abwärme über Pins 17 bzw. 18, die hier J-förmig ausgeführt sind, in die externe Leiterplatte, auf welche das Multi-Chip-Modul montiert wird. Gleichzeitig dienen die Anschlußelemente 11 und 12 mit ihren Pins 17 bzw. 18 selbst als Kühlkörper.

Es wird darauf hingewiesen, daß **Fig. 1** nicht maßstabsgetreu gezeichnet ist. Lediglich zur besseren Anschaulichkeit ist die Dicke der einzelnen Lagen im Verhältnis zur Breite erheblich vergrößert.

Funktionen des Trägersubstrats 1 sind im wesentlichen eine Erhöhung der Stabilität der internen Leiterplatte sowie eine Verbesserung der Wärmeableitung zu den Anschlußelementen 11 und 12. Werden durch die verwendeten Verfahren zur Fertigung des Multi-Chip-Moduls oder durch dessen Handhabung geringere Anforderungen an die Stabilität gestellt, so kann auch auf ein Trägersubstrat verzichtet werden. Das Trägersubstrat kann auch durch eine Lage aus gut wärmeleitendem Material, beispielsweise Metall, ersetzt werden. Dies wirkt sich vorteilhaft auf die Dicke der internen Leiterplatte und somit auf die Bauhöhe des Multi-Chip-Moduls mit einer derartigen Leiterplatte aus.

Wie in dem Schnittbild nach **Fig. 2** dargestellt, wird eine interne Leiterplatte 19 sowohl auf ihrer Oberseite als auch auf ihrer Unterseite mit einem Halbleiterbauelement 20 bzw. 21 bestückt. Die elektrischen Verbindungen zwischen Anschlußflächen der Halbleiterbauelemente und Anschlußflächen auf der internen Leiterplatte 19 sind durch Bonden mit Bond-Drähten 22 hergestellt. Das Multi-Chip-Modul ist in einem Gehäuse 23 aus einer Vergußmasse, beispielsweise aus Plastik, gegen mechanische und chemische Beanspruchungen geschützt. Aus dem Gehäuse 23 ragen Pins 24 und 25 heraus, die durch Lot elektrisch mit einer externen Leiterplatte 26 verbunden sind, auf welcher das Multi-Chip-Modul montiert ist. Werden nur geringe Anforderungen an den Schutz vor Umwelteinflüssen gestellt, so kann das Gehäuse auch offen ausgeführt werden und beispielsweise als Trägerrahmen dienen oder ganz entfallen.

Alternativ zur in **Fig. 2** gezeigten Bond-Verdrahtung können Anschlußflächen von Halbleiterbauelementen auch als Metallisierung ausgeführt werden, die sich auf den Kanten oder auf der Unterseite des Halbleiterbauelements, die der internen Leiterplatte im bestückten Zustand zugewandt ist, befinden und direkt mit Anschlußflächen der internen Leiterplatte verlötet werden. Diese Ausführungsform zeichnet sich durch eine geringere Bauhöhe aus, da kein Raum für die Bond-Verdrahtung benötigt wird.

In der Explosionsdarstellung nach **Fig. 3** sind zwei interne Leiterplatten 27 und 28, die mit Halbleiterbauelementen 29, 30 bzw. 31, 32 beidseitig bestückt sind, übereinander angeordnet. Darunter befindet sich eine Leiterplatte 33, auf welche das fertigmontierte Multi-Chip-Modul bestückt werden kann. Die Halbleiterbauelemente 29...32 sind hier mit Anschlußelementen versehen, die als Metallisierung des Halbleitermaterials ausgeführt sind. In **Fig. 3** sind davon lediglich einige Anschlußelemente der Halbleiterbauelemente 29 und 31, beispielsweise ein Anschlußelement 34, sichtbar. Die internen Leiterplatten 27 und 28 besitzen hierzu korrespondierende Anschlußflächen 35, die mit Lot gefüllt sind, damit die Halbleiterbauelemente 29 ... 32 direkt mit den internen Leiterplatten 27 und 28 verlötet werden können. Durchkontaktierungen 36 dienen zur Wärmekopplung der Halbleiterbauelemente 29 ... 32 über die internen Leiterplatten 27 und 28 hinweg, so daß eine in einem der Halbleiterbauelemente 29, 30, 31 oder 32 entstehende Abwärme sich gleichmäßig auf den Bauelementestapel verteilt und nicht zu einer punktuellen Erhitzung führt. Die Leiterplatten 27 und 28 sind mit internen Metallagen zur Entwärmung versehen und liefern so beide einen Beitrag zur Entwärmung des Bauelementestapels. Für eine weitere Verbesserung der Wärmekopplung können die Durchkontaktierungen 36 auch mit einem Wärmeleiter, insbesondere einer Wärmeleitpaste, ausgefüllt werden. Für eine elektrische und wärmeleitende Verbindung ist die interne Leiterplatte 28 mit Anschlußelementen 37 versehen, die mit zu diesen korrespondierenden Anschlußflächen 38 auf der internen Leiterplatte 27 verlötet werden. Ebenso sind entlang der Kanten der internen Leiterplatte 27 Anschlußelemente 39 angeordnet, die mit Anschlußflächen 40 der externen Leiterplatte 33 verlötet werden.

In einer anderen, in den Figuren nicht dargestellten Ausführungsform können die Anschlußelemente von übereinander angeordneten internen Leiterplatten auch vertikal fluchtend plaziert werden, so daß die Anschlußelemente benachbarter interner Leiterplatten direkt miteinander verlötet werden. Diese Bauform bietet sich insbesondere dann an, wenn gleiche Halbleiterbauelemente gestapelt werden, da auf diese Weise gleiche interne Leiterplatten für die verschiedenen Ebenen verwendet werden können.

Alternativ zu dem in **Fig. 3** gezeigten Ausführungsbeispiel kann anstelle der Durchkontaktierungen zur Wärmekopplung auch jeweils eine Aussparung in den internen Leiterplatten vorgesehen werden, welche im wesentlichen den Raum zwischen den Anschlußflächen 35 einnimmt und mit einem gut wärmeleitenden Material, beispielsweise einer Metallplatte, ausgefüllt wird.

Der neue Stapelaufbau eines Multi-Chip-Moduls erlaubt in vorteilhafter Weise auch, auf der Oberseite des Multi-Chip-Moduls einen Kühlkörper anzuordnen, der thermisch mit dem Bauelementestapel gekoppelt wird.

Vorteilhaft auf die Wärmeableitung über die Anschlußelemente des Multi-Chip-Moduls zur externen Leiterplatte hin wirkt sich auch die geringe Dicke der Verdrahtungsschicht aus, welche die Anschlußelemente von den innerhalb der internen Leiterplatte eingebetteten Metallagen elektrisch isoliert. Die Verdrahtungsschichten mit einer geringeren Wärmeleitfähigkeit stellen somit einen nur vergleichsweise kurzen Weg für die Abwärme dar und verringern kaum den über die Anschlußelemente übertragbaren Wärmestrom.

In einer weiteren von **Fig. 3** abweichenden Bauform können obere interne Leiterplatten auch größer als untere ausgeführt und mit längeren Anschlußelementen versehen werden, welche die unteren internen Leiterplatten seitlich überragen und direkt mit der externen Leiterplatte verlötet werden. Die Anordnung der Anschlußflächen auf einer externen Leiterplatte ähnelt dann einem Rasterfeld mit mehreren Anschlußreihen.

Für die beidseitige Bestückbarkeit der internen Leiterplatten sollten diese mehrlagig ausgeführt werden, damit bei gleichen Halbleiterbauelementen die spiegelbildliche Anordnung der Bauelementeanschlüsse auf ein gemeinsames Anschlußschema für das Multi-Chip-Modul zurückgeführt werden kann.

Das neue Multi-Chip-Modul ist aufgrund seiner hohen Packungsdichte beispielsweise in den folgenden An-